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Patent Amendment

REMARKS

This application has been carefully reviewed in light of the Office Action dated September 21, 2005. Claims 1 and 13 are amended. Reconsideration and favorable action in this case are respectfully requested based on the reasons set forth below.

The Examiner has rejected claims 1, 4-6, 8, 10, 11, 13, 14 and 17-19 under 35 U.S.C. §103(a) as being unpatentable over DeRoo in view of U.S. Pat. No. 6,016,525 to Corrigan. Applicants have reviewed these references in detail and do not believe that they disclose or make obvious the invention as claimed.

The Examiner has rejected claims 2, 3, 7, 9, 12, 15, 16 and 20 under 35 U.S.C. §103(a) as being unpatentable over DeRoo in view Corrigan and further in view of U.S. Pat. No. 5,887,146 to Baxter. Applicants have reviewed these references in detail and do not believe that they disclose or make obvious the invention as claimed.

Claims 1 and 8 were amended to correct a grammatical error.

With regard to claims 1, 8 and 13, Applicant maintains its position, previously stated, that DeRoo does not show circuitry for receiving a signal specifying a normal mode or a verification mode. The passages cited by the Examiner in support of showing this feature do not describe anything similar to a verification mode signal.

The Examiner admits that DeRoo does not explicitly state selectively passing system memory accesses either to the system memory or the shared memory responsive to the signal, wherein accesses directed towards the system memory are passed to the system memory in a normal mode and wherein accesses directed towards the system memory are passed to the shared memory in a verification mode. The Examiner uses the Corrigan reference to provide this teaching state that Corrigan explicitly discloses this feature as his system provides loopback testing wherein a signal directed towards overlapping address space is passed to a shared memory.

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Applicant has reviewed Corrigan in detail and does not agree with the Examiner's conclusions as to its teachings. As will be described in detail below, Corrigan shows the ability to access a shared memory 202 in one of two ways. First, the shared memory 202 can be accessed in a normal fashion over the primary PCI bus 252. Second the shared memory 202 can be accessed over the following path: PCI Bridge (Primary interface) 2, pad flow circuit 6, pad 8, pad flow circuit 6 (a second time), shared memory bridge 4, and shared memory bus 250. The purpose of using the second path is to test the circuitry in the PCI bridge 2 and shared memory bridge 4.

More specifically, the PCI bridge 2 in Corrigan allows devices on the secondary PCI bus 256 to communicate with devices on the primary PCI bus 252, and vice versa (col. 4, lines 135-54). The shared memory bridge 4 allows device on the secondary PCI bus 256 to read and write to the shared memory 202 (col. 5, lines 10-20).

Each bridge 2 and 4 recognizes data transfers requiring its attention based on the address supplied in the transfer request. The PCI bridge 2 uses an address range specified in the secondary address register 12 and the shared memory bridge 4 uses an address range specified in the shared memory address register 14. If the address ranges in these two registers overlap (loopback mode), and a transfer request on the primary PCI bus 252 specifies an address within the overlapping range, the following will occur: (1) the PCI bridge 2 will see this as a request to access a device on the secondary bus 256 through the PCI bridge 2; the request will thus be translated and placed on the secondary bus 256 and (2) the shared memory bridge 4 will see the translated request as a request to access shared memory 202, and will thus translate the request back to the protocol used on the primary PCI bus to access the shared memory (col. 6, lines 6-27). This path is shown in Figures 2 and 3 of Corrigan.

Accordingly, Corrigan shows two *paths* available for a device on the primary bus 252 to access a *single* shared memory 202. A device on the primary PCI bus can thus

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access the shared memory either directly over the primary PCI bus or indirectly via the secondary PCI bus and the two bridges 2 and 4. Corrigan does *not*, however, teach selectively passing memory accesses intended for a system memory to either a system memory or an internal shared memory responsive to a verification mode signal.

If DeRoo were combined with Corrigan, it would only result in a DeRoo having a master processor that could access a single memory using one of two possible paths. Any transfer request intended for the shared memory would eventually access the shared memory regardless of whether the device was in loopback mode – the only difference would be which path was used to get to the shared memory. Corrigan does not provide for an access to a system memory resulting in the access of another, internal, memory. Thus, it would not be able to provide the debugging capabilities of the present invention, because it does not have the capability to selectively re-direct memory access requests intended for the system memory to a shared memory in the slave processor subsystem while in a verification mode. In the present invention, a slave processor that normally writes to an external system memory associated with a master processor can write (in verification mode) to an internal shared memory. Thus, in verification mode in the present invention, the slave processor subsystem can be completely isolated from the master processor subsystem. This is not true of the combination of DeRoo and Corrigan.

Because of the foregoing, Applicants request allowance of independent claims 1, 8 and 13, and dependent claims 2-7, 9-12, and 14-20

An extension of one month is requested and a Request for Extension of Time under § 1.136 with the appropriate fee is attached hereto.

The Commissioner is hereby authorized to charge any fees or credit any overpayment, including extension fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.


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Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Alan W. Lintel, Applicants' Attorney at (972) 664-9595 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



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